What is claimed is:

1. A method of fabricating a metal oxide semiconductor field effect transistor (MOSFET), comprising:

providing a substrate comprising a layer of strained silicon grown on a layer of silicon germanium, and shallow trench isolations defining active regions of the substrate for formation of respective MOSFET devices;

implanting carbon into the strained silicon of an active region; and

forming a MOSFET that incorporates the carbon implanted strained silicon layer in said active region.

2. The method claimed in claim 1, wherein the implanted carbon increases a tensile strain of the strained silicon layer in said active region.

3. The method claimed in claim 1, wherein a PMOS device is formed in said active region, and wherein an NMOS device that incorporates the strained silicon layer is formed in an active region that is not implanted with carbon.

4. The method claimed in claim 1, wherein implanting carbon comprises:

forming a photoresist mask that leaves said active region exposed;

implanting said carbon using the photoresist mask as an implant mask; and

removing the photoresist mask.

5. The method claimed in claim 1, wherein the silicon germanium layer has a composition $Si_{1-x}Ge_x$, where x is in the range of 0.1 to 0.3.

6. The method claimed in claim 1, wherein forming said MOSFET comprises:

forming a gate insulating layer on the strained silicon layer;

forming a gate conductive layer on the gate insulating layer; and

patterning the gate conductive layer and the gate insulating layer to form a gate overlying a gate insulator.

7. The method claimed in claim 6, wherein forming said MOSFET further comprises:

forming a protective layer around the gate; and

implanting shallow source and drain extensions.

8. The method claimed in claim 7, wherein implanting shallow source and drain extensions is preceded by implanting halo regions, the halo regions extending toward a channel region beyond ends of the source and drain extensions to be formed, the halo regions comprising a dopant having a conductivity type opposite to the conductivity type of a dopant of the source and drain extensions.

9. The method claimed in claim 7, wherein forming the MOSFET further comprises:

forming a spacer around the gate; and

implanting deep source and drain regions,

wherein the spacer serves as an implantation mask during implanting of the deep source and drain regions.

10. The method claimed in claim 9, wherein forming the MOSFET further comprises:

forming silicide source and drain contacts and a silicide gate contact.

11. The method claimed in claim 10, wherein the silicide source and drain contacts and the silicide gate contact comprise nickel.

12. The method claimed in claim 11, wherein forming silicide source and drain contacts and a silicide gate contact is preceded by annealing to activate implanted dopants.

13. The method claimed in claim 1, wherein providing the substrate comprises growing the layer of silicon germanium on a semiconductor substrate.

14. The method claimed in claim 13, further comprises growing the layer of strained silicon on the layer of silicon germanium.

15. The method claimed in claim 14, wherein the layer of silicon germanium and the layer of strained silicon are grown together in a single continuous in situ deposition process.

16. A method of fabricating metal oxide semiconductor field effect transistors (MOSFETs), comprising:

providing a substrate comprising a layer of silicon germanium and a layer of strained silicon grown on the layer of silicon germanium, and shallow trench isolations defining respective active regions of the substrate for formation of NMOS and PMOS devices;

selectively implanting carbon into the strained silicon of the PMOS active regions using the mask as an implant mask; and

forming PMOS devices and NMOS devices that incorporate the strained silicon in the respective PMOS and NMOS active regions of the substrate.

17. The method claimed in claim 16, wherein the implanted carbon increases a tensile strain of the strained silicon layer.

18. The method claimed in claim 16, wherein a hole mobility in carbon implanted strained silicon of said PMOS devices is approximately equal to an electron mobility in strained silicon of said NMOS devices having no implanted carbon.

19. The method claimed in claim 16, further comprising electrically connecting one of said PMOS devices and one of said NMOS devices to form a CMOS device.

20. The method claimed in claim 16, wherein selectively implanting carbon is preceded by masking active regions for NMOS devices using a photoresist mask, and

wherein selectively implanting carbon is followed by removing the photoresist mask.

21. A metal oxide semiconductor field effect transistor (MOSFET) device comprising:

source and drain regions;

a channel region extending between the source and drain regions;

a gate insulator overlying the channel region; and

a gate overlying the gate insulator,

wherein the source and drain regions are formed in a semiconductor material comprising a strained silicon layer grown on a silicon germanium layer that imparts tensile strain to the strained silicon layer, and

wherein the layer of strained silicon has carbon incorporated therein to impart an additional tensile strain.

22. The device claimed in claim 21, wherein the silicon germanium layer has a composition $Si_{1-x}Ge_x$ where x is in the range of 0.1 to 0.3.

23. The device claimed in claim 21, wherein the MOSFET device is a silicon on insulator (SOI) device.

24. A complementary metal oxide semiconductor field effect transistor (CMOS) device comprising a PMOS device electrically connected to an NMOS device,

wherein the PMOS device and the NMOS device each comprise sources and drains formed in a semiconductor material comprising silicon germanium having a layer of strained silicon grown thereon, and

wherein the strained silicon of the PMOS device has carbon incorporated therein to impart an additional tensile strain.

25. The device claimed in claim 24, wherein the silicon germanium layer has a composition $Si_{1-x}Ge_x$ where x is in the range of 0.1 to 0.3.

26. The device claimed in claim 24, wherein the CMOS device is a silicon on insulator (SOI) device.